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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/669,411	09/25/2003	Shoji Otaka	243021US2RD	5047

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EXAMINER	
JACKSON, BLANE J	

ART UNIT	PAPER NUMBER
2685	

DATE MAILED: 01/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/669,411	OTAKA, SHOJI	
	Examiner	Art Unit	
	Blane J. Jackson	2685	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15 and 17-23* is/are rejected.

7)☒ Claim(s) *16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 September 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 3-5 and 22 are rejected under 35 U.S.C. 102(e) as being anticipated by Tiller (US 6,529,721).

As to claims 1 and 3, Tiller teaches a frequency converter comprising:

A transconductance unit that outputs a first output signal based on an input signal having a first frequency (figure 6, single ended RF input stage based on transistor (50), first output to transistor pair (60 and 62), column 3, lines 23-27),

An impedance matching unit that includes a least one inductor through which the first output signal passes (transistor pair emitters (64) couple through the inductive leg (52B) of balun (52) to signal ground with the leg in parallel with split capacitor (90), column 3, lines 28-39 and column 4, lines 54-64),

A current switching unit that converts the fist output signal output from the impedance matching unit to a second output signal having a second frequency based on a local oscillator signal (figures 2-6, Gilbert cell, column 3, lines 40-48).

As to claim 22 with respect to the claim elements of claim 1, Tiller teaches an integrated double balanced radio mixer for up and/ or down frequency conversion with application to cellular communications and cordless telephony, column 1, lines 5-29.

As to claim 4 with respect to claim 1, Tiller teaches the transconductance unit includes a first transistor wherein the input signal is input to a base of the first transistor and the first output signal is output from a collector of the first transistor (transistor (50), figures 2-6),

The current switching unit includes second and third transistors wherein the first output signal output form the impedance matching unit is input to emitters of the second and third transistors and the local oscillator signal is applied between bases of the second and third transistors (Gilbert cell, second transistor (60) and third transistor (62)).

As to claim 5 with respect to claim 4, Tiller teaches the impedance matching unit comprises:

A first capacitor having two terminals, one terminal being connected to the emitters of the second and third transistors and another terminal being connected to the earth (figure 6, capacitor (90) would be split, column 4, lines 54-64, the second terminal of each coupled to earth ground through connection (52C) and capacitor (54)),

A second capacitor having two terminals, one terminal being connected to the collector of the first transistor and another terminal being connected to earth (capacitor (92) connected to earth via capacitor (54)),

An inductor having two terminals, one terminal being connected to the emitters of the second and third transistors and another terminal being connected to the collector of the first transistor (transformer section (52B) with connection (64) to second and third transistors and "connected" or coupled to transistor (50) collector via transformer (52).

2. Claims 11, 12, 14, 15 and 23 are rejected under 35 U.S.C. 102(e) as being anticipated by Yan et al. (US 6,819,914).

As to claim 11, Yan teaches a frequency converter comprising:

A first transconductance unit that outputs a first output signal based on a first input signal having a first frequency (figure 2, first transconductance unit based on transistor (52)),

A first impedance matching unit that includes at least one first inductor through which the first output signal passes (relative portion of transformer (58)),

A first current switching unit that converts the first output signal output form the first impedance matching unit to a second output signal having a second frequency based on a local oscillator signal (Gilbert cell transistor pair (66) and (68)),

A second transconductance unit that outputs a first output signal based on a first input signal having a first frequency (figure 2, second transconductance unit based on transistor (50)),

A second impedance matching unit that includes at least one second inductor through which the third output signal passes (relative portion of transformer (58)),

A second current switching unit that converts the first output signal output form the first impedance matching unit to a second output signal having a second frequency based on a local oscillator signal (Gilbert cell transistor pair (70) and (72), column 3, line 44 to column 4, line 34).

As to claim 23 with respect to the claim elements of claim 11, Yan teaches a differential receiver front end section comprising a low noise amplifier and frequency conversion mixer, figure 2, column 3, line 44 to column 4, line 34 applicable to up and down conversion in a wireless transceiver, figure 1, column 2, line 55 to column 3, line 43.

As to claim 12 with respect to claim 11, Yan teaches a current source that is commonly connected to the first and second transconductance units (figure 2, primary bias (60)).

As to claim 14 with respect to claim 11, Yan teaches each of the fist and second impedance matching units includes further at least one capacitor (figure 2, capacitor (64)).

As to claim 15 with respect to claim 11, Yan teaches the first transconductance unit includes a first transistor wherein the first input signal is input to a base of the first

transistor and the first output signal is output from a collector of the first transistor (figure 2, RF input with collector output of transconductance transistor (52)),

The first current switching unit includes second and third transistors (transistors (66 and 68)), wherein the first output signal output from the first impedance matching unit is input to emitters of the second and third transistors and the local oscillator signal is applied between bases of the second and third transistors (figure 2, quadrature mixer, LO (74)),

The second transconductance unit includes a fourth transistor, wherein the second input signal is input to a base of the fourth transistor and the first output signal is output from a collector of the fourth transistor (figure 2, RF input with collector output of transconductance transistor (50)),

The second current switching unit includes fifth and sixth transistors (transistors (70 and 72)), wherein the third output signal output from the second impedance matching unit is input to emitters of the fifth and sixth transistors and the local oscillator signal is applied between bases of the second and third transistors (figure 2, quadrature mixer, LO (74)),

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tiller (US 6,529,721) with a view to Long (US 6,026,286).

As to claims 2, 6 and 7, Tiller teaches various mixer configurations to improve linearity and noise figure, column 4, line 65 to column 5, line 6, where the circuits are implemented in the integrated circuit, column 2, lines 58-67 but is silent on application of the inductor is formed as part of a monolithic integrated circuit.

Long teaches a mixer configuration similar to Tiller to improve the noise figure, reduce thermal noise and for operation with lower supply voltage and does so in view of bipolar CMOS technology for a MMIC with specific attention to a monolithic microstrip transformer, the balun for splitting the RF signal in the transconductance unit, figure 5, transformer (513), column 3, lines 15- 65.

It would have been obvious to one of ordinary skill in the art at the time of the invention to realize the mixer circuit of Tiller fabricated as a monolithic integrated circuit as taught by Long to for significant performance improvements over broadband designs.

4. Claims 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tiller (US 6,529,721).

As to claims 8-10 with respect to claim 7, Tiller teaches the parallel resonant circuit has a resonance frequency that is tuned, column 4, lines 54-64, but does not specifically discloses the resonant circuit is tuned to two or more times the frequency of the local oscillator signal. However, Tiller also teaches the resonant circuit may be tuned to provide additional image noise rejection, therefore, it would have been obvious

to one of ordinary skill in the art at the time of the invention to consider the tuning approach of Tiller to tune the resonant circuit to block any desired RF frequency to improve the noise figure of the mixer.

5. Claims 13 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yan et al. (US 6,819,914) with a view to Long (US 6,026,286).

As to claims 13 and 17 with respect to claims 11 and 14, Yan teaches a fully differential receiver front end section including a quadrature mixer, column 3, lines 44-57, where the circuit is based on PMOS or NMOS transistors, column 2, lines 1-24, but is silent on application of the first and second inductors are formed as part of a monolithic integrated circuit.

Long teaches a mixer configuration similar to Tiller to improve the noise figure, reduce thermal noise and for operation with lower supply voltage and does so in view of bipolar CMOS technology for a MMIC with specific attention to a monolithic microstrip transformer, the balun for splitting the RF signal in the transconductance unit, figure 5, transformer (513), column 3, lines 15- 65.

It would have been obvious to one of ordinary skill in the art at the time of the invention to realize the mixer circuit of Yan fabricated as a monolithic integrated circuit as taught by Long to for significant performance improvements over broadband designs.

6. Claims 18-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yan (US 6,819,914) with a view to Long (US 6,026,286).

As to claim 18 with respect to claim 14, Yan teaches a quadrature mixer comprising a differential transconductance circuit coupled to a double balanced mixer core via a first and second impedance matching circuit (figure 2) but does not teach the first and second impedance matching units is a parallel resonant circuit that includes the inductor and capacitor wherein the inductor and capacitor are formed as a part of a monolithic integrated circuit.

Long teaches a quadrature mixer comprising a first and second impedance matching units as a parallel resonant circuit that includes the inductor and capacitor wherein the inductor and capacitor are formed as a part of a monolithic integrated circuit (figure 2, column 3, lines 19-42, transformer portion (516) in parallel with capacitor (534) and transformer portion (518) in parallel with capacitor (536)).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the mixer circuit of Yan with the impedance matching circuit of Long comprising capacitors to tune the circuit to lower the noise figure.

As to claims 19-21 with respect to claim 18, Long of Yan modified teaches the parallel resonant circuit has a resonance frequency that is tuned, column 3, lines 33-42, but does not specifically discloses the resonant circuit is tuned to two or more times the frequency of the local oscillator signal. Long teaches the additional parallel capacitors in context with lowering the noise figure, therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to consider the tuned circuit of Yan modified to block any desired RF frequency to improve the noise figure of the mixer.

Allowable Subject Matter

7. Claim 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Wu et al. (US 6,653,885), Hareraats (US 6,704,559), Schiltz (US 6,665,527), Wyse (6,230,001) and Nguyen (US 5,379,457).

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Blane J. Jackson whose telephone number is (571) 272-7890. The examiner can normally be reached on Monday through Friday, 8:00 AM-5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward Urban can be reached on (571) 272-7899. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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